PTO/SB/08B (10-01)
Approved for use through 10/31/2002. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449B-PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet | 1 | | 1

Complete if Known	
Applicati n Number	09/330,231
Filing Dat	Jun 10, 1999
First Named Inventor	Roberto Passerone
Art Unit	2181
Examiner Name	Justin King
Attorney Docket No.	248/248; 2195357051

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher city and/or country where published
	1	Aho, A. V. et al. "Compilers Principles, Techniques and Tools," *Addison-Wesley,* pp. 83, 94-98, 107, 113, 120-125, 129, 135-141, 148, 172-173, 268-269, Reading, MA, 1988.
	2	Akella, J. et al. "Synthesizing converters between finite state protocols," *Proceedings of the International Conference on Computer Design,* pp. 410-413, Cambridge, MA, October 15-15, 1991.
	3	Alfaro, L., et al. "Interface Theories for Component-based Design," University of California, Santa Cruz, *University of California, Berkeley,* (EMSOFT), 2001 (19 pp).
	4	Alfaro, L., et al. "Interface Automata," *Dept. of Electrical Engineering and Computer Sciences, University of California, Berkeley,* (FSE), 2001 (17 pp).
	5	Borriello, G. "A new Interface Specification Methodology and its Applications to Transducer Synthesis," *Ph.D. thesis, University of California at Berkeley,* pp. 116-136, Berkeley, CA, 1988.
	6	Borriello, G. et al. "Synthesis and optimization of interface transducer logic," *Proceedings of the International Conference on Computer Aided Design,* pp. 274-277, November 1987.
	7	Brzozowski, J. A.. "Derivatives of regular expressions," *Journal of the Association for Computing Machinery,"* 11(4): pp. 481-494, October 1964.
	8	Burch, J.R., et al. "Modeling Hierarchical Combinational Circuits" *IEEE1063-6757/93* pp. 612-617 1993.
	9	Coelho, C. N. et al. "Analysis and synthesis of concurrent digital circuits using control-flow expressions," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,"* 15(8): pp. 854-876, August 1996.
	10	Filo, D. et al. "Interface Optimization for Concurrent Systems Under Timing Constraints," *1 IEEE Transactions on VLSI Systems,* pp. 172-185 (Sept. 1993).
	11	Hopcroft, J. E. et al. "Introduction to Automata Theory, Languages, and Computation," *Addison Wesley,* pp. 19-46, 217-220, 250-253, Reading, MA, 1986.
	12	Narayan, S. et al. "Interfacing Incompatible protocols using interface process generation," *Proceedings of the 32nd Design Automation Conference,"* pp. 468-473, San Francisco, CA, June 12 – 16, 1995.
	13	Öberg, J. et al. "Grammar-based hardware synthesis of data communication protocols," *Proceedings of the 9th International Symposium on System Synthesis,"* pp. 14-19, La Jolla, CA, November 5-8, 1996.
	14	Passerone, R. "Automatic Synthesis of Interfaces between Incompatible Protocols," M.S. Thesis, University of California at Berkeley, 1997.
	15	Passerone, R., et al. "Convertibility Verification and Converter Synthesis: Two Faces of the Same Coin," Cadence Berkeley Laboratories; University of California, Santa Cruz; University of California, Berkeley. 2002
	16	Rowson, J. A. et al. "Interface-based design," *Proceedings of the 34th Design Automation Conference,* pp. 178-183, Anaheim, CA, June 9 – 13, 1997.
	17	Seawright, A. et al. "Clairvoyant: A synthesis system for production-based specification," *IEEE Transactions on VLSI Systems,* 2: pp. 172-185, June 1994.
	18	Sun, J. S. et al. "Design of system interface modules," *Proceedings of International Conference on Computer Aided Design,* pp. 478-481, 1992.

Examiner's Signature	Justin King	Date Considered	4.10.03	

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.